REMARKS

Claim Rejections -35 USC §112

The rejection includes:

> "Claims 63, 67, 72, 77, 81, and- 86 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
>
> Regarding claim 63, lies (sic) 2-4 is unclear. What does applicant mean of "second edge of the trace and first edge of the second cap are both substantially equal to X"? Does applicant mean either the dimension or size of the second edge of the trace and -the first edge of the second cap are both substantially equal to X (0.1 in).
>
> Rejected claims 67, 72, 77, and 88 are similar to claim 63.
>
> Please clarify."

The issue raised by the Examiner seeks the meaning of a claim phrase. It is submitted that the language quoted is already clear when considered in the context in which it appears (the rest of the sentence/claim) particularly by referring to Figure 1 of the drawing.

The entire claim 63 is:

63. The circuit protection system as described in claim 62 wherein **the dimension of the space intermediate**
(1) said first edge of said trace and said first edge of said first end cap and
(2) said second edge of said trace and said first edge of said second end cap

are both substantially equal to X. (emphasis added)

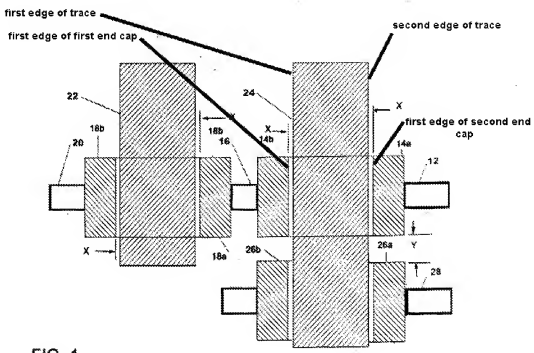


FIG. 1

The marked up copy of Fig. 1 of the drawing above is provided to emphasize that which is shown in the drawing including the explicitly labeled dimension. It will be understood that "X" is used to refer the dimension of the space intermediate both a first set of two edges as well as the dimension of the space intermediate a second set of two edges.

The term "X" is used in the same sense that it is used in elementary algebra. See http://www.newton.dep.anl.gov/askasci/math99/math99228.htm
http://www.garlikov.com/math/UnderstandingAlgebra.html

As used in claim 63 the dimension is an unspecified quantity, however, the claims make clear that both of the respective dimensions are substantially equal to X. Thus, the first and second dimensions are inherently substantially equal to each other. The use of the standard algebraic representation in claim 63 facilitates subsequent more specific

claims. Claim 63 further limits claim 62 because it specifies that two specific dimensions are substantially equal. Claim 65 is a more specific claim that specifies that the two recited dimensions are both substantially equal to each other and substantially equal to .01 inch.

It is respectfully submitted that the asserted issue relates to specific words out of the context in which they appear. More specifically, the words referred to by the Examiner have been removed from the sentence (the claim) in which they appear and then challenged as not having meaning independent of the rest of the sentence. The words when taken in context are fully supported by both the original specification and the specification as amended in the response dated 10/11/06. See specifically, page 8 of the specification.

Claim Rejections -35 USC §103(a)

The rejection is:

> 4. Claims 62-70,76-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Laschinski (U.S. Patent 6,467,163) in view of Tanabe et al. (U.S. Patent 4,883,920).
>
> **As to claims 62, 76, Laschinski discloses a universal component mounting structure for surface mountable electronic devices as shown in figures 1-2 comprising:**
>
> **a printed circuit board (2, column 3, lines 60-61) having a SMT component (16) mounted on, the component (30; 40) having first and second terminals (column 5, lines 23-24), and each terminals having a first edge;**
>
> **a conductive trace (10) formed on the PCB (2) having first and second opposed edges extending intermediate said first and second terminals (see figure 2), the edges of the trace (10) being defined a plane, see figure 2 and intersecting the first edge of the first and second terminals, the edge of the trace (10) disposed in parallel spaced relative to the edge of the first and second terminals respectively.**
>
> Laschinski does not specifically disclose the SMT component (16) having end caps. Tanabe et al. teaches a SMT component (2) having end caps (4) mounted on a substrate (1). It would have been obvious to one having an ordinary skill in the art at the time the invention was made to have the SMT component having end caps as taught by Tanabe et al. employed the SMT component of Laschinski in order to easy install components mounted on the PCB.

As to claims 66, 80, Laschinski discloses a universal component mounting structure for surface mountable electronic devices as shown in figures 1-2 comprising:

a printed circuit board (2, column 3, lines 60-61) having a first SMT component (16) mounted on, the component (30; 40) havinq first and second terminals (column 5, lines 23-24), and each terminals having a first edge; and a second SMT component (14) having end caps (see figure 2), and a conductive trace (10) formed on the PCB (2) having first and second opposed edges extending intermediate said first and second terminals (see figure 2), the edges
of the trace (10) being defined a plane, see figure 2 and intersecting the first edge of the first and second terminals, the edge of the trace (10) disposed in parallel spaced relative to the edge of the first and second terminals respectively.

Laschinski does not specifically disclose the SMT component (16) having end caps. Tanabe et al. teaches a SMT component (2) having end caps (4) mounted on a substrate (1). It would have been obvious to one having an ordinary skill in the art at the time the invention was made to have the SMT component having end caps as taught by Tanabe et al. employed the SMT component of Laschinski in order to easy install components mounted on the PCB." (Emphasis added)

The bold font words above is materially incorrect with respect to the word "intermediate". The structure provides a printed circuit board that include planar conductive traces positioned for contact with the planar faces of the terminals of the surface mounted component. The lower face of the surface mounted component (that includes the lower face of the respective terminals) are thus in a different plane than the plane defined by the conductive traces. The respective planes are not even in face to face abutting relationship. They are spaced apart by the thickness of the solder intermediate the terminals and the plane of the conductive traces. There is no plane defined by the edges of end caps as specified in the claims that extends through the land 10.

In addition to the above noted imprecision the follow issues relating to the rejection are also noted:

1. Neither reference relied on relates to the problem of transient protection or dissipating transients or even mentions the word "transients" or any synonym thereof.

2. Neither reference relied on relates to any solution for dissipating transients.

3. Laschinski teaches that land 10 is only for attachment of device terminals.

4. Laschinski teaches that the sizing and location of lands is based solely on the dimensions of the family of surface mounted devices to which the surface mounted component is to be attached and insulating gap requirements. See the paragraph bridging columns 2 and 3: "For example, a few industry standard sizes for surface mount resistors and capacitors are commonly know as 805,1206, and 1210, the sizes being 0.080xO.050 in., and 0.120xO.060 in., and 0.120xO.100 in. respectively. The terminations or connection points on these examples are on the ends of the longer axis. For a universal mounting 5 pattern to accommodate placement of anyone of these example devices, an insulating gap of 0.070 in. or less between the two conductive lands and the combined widths of the lands and the insulating gap are at least 0.130 in. or more is required. Multiple variations of circuit land and gap 10 patterns base on the above mentioned concept can then be combined on a common printed circuit structure to provide a proto typing breadboard if so desired. Three terminal devices can also be accommodated by designing land patterns comprised of two or more parallel and one or more 15 perpendicular conductive circuit lands with the insulating gaps between the lands."

5. Laschinski teaches only a prototyping board only for mounting surface mounted components. See Figure 6 illustrating in-line connectors for making connections to the respective surface mount components on the prototyping board.

6. Laschinski does not teach a land that is intermediate the edges of respective end caps of the same surface mounted component.

7. The placement of all lands, including land 10, in Laschinski is determined based on the spacing required by respective families of surface mounted components. There is no suggestion that the spacing should be governed by the need for dissipating transients or even of the dimensions intermediate respective lands on the board.

8. Laschinski in addition to not describing surface mount components that include end caps, clearly does not describe or even mention the dimensions X and t dimensions as defined in the present specification and claims of the present application much less identify the importance of these dimensions in any embodiment in the reference.

9. Laschinski is so totally unconcerned about transients that the specification of that reference refers almost as an afterthought to the connection of power to the board. See column 7, final paragraph:

> "As shown in FIG. 3, interconnection of other circuits to the universal mounting structure for surface mountable electronic devices in any of its possible configuration within the context of the present invention described above can take a variety of forms. The wires 70, leads, terminal, or other electrically conducting objects of other circuits 72 that are to be connected can be soldered directly to the circuit lands, or could be attached by bonding to the circuit lands with conductive adhesives or by the use of welding. Any means that provide an electrical connection that meets the requirements of the circuit designer would be appropriate. Another method of interconnection would be the use of a socket or edge card connector, in which case the present invention could be modified so as to have one or more edges provided with a circuit pattern that can interface with said socket or connector."

10. Even if the Examiner's conjuncture about it being obvious to combine Laschinski and Tanabe were correct, the combination would still not suggest anything relating to dissipating transients.

11. It is recognized KSR v. Teleflex 550 U.S. 398, 1275 S. Ct 1727 (2007) allows patent examiners to look at art other than art specifically directed to the problem the patentee was trying to solve. Even in KSR, the examiner found art related to brakes. In contrast, the references relied on in the present case have nothing to with transient dissipation.

12. The references relied on do not constitute provide factually supported objective evidence establishing a *prima facie* case of obviousness. The only possible manner in which the combination of these references would show or suggest, to a person having ordinary skill in the art, the present invention is by the use of impermissible hindsight. Because the references have no relevance to transient dissipation, it is inescapable that that the present application has been merely used to apply hindsight as abundantly described in many references:

http://www.patentlyo.com/patent/2006/11/hindsight_bias.html

http://www.patenthawk.com/blog/2006/08/impermissible_hindsight_1.html

Thus, the references either alone or in combination do not have the structure explicitly claimed, do not have the purpose of the present invention (either intentionally or inherently), and do not achieve the result of the present invention either intentionally or inherently. Accordingly, there is no rational, good faith, plausible, or credible support for rejection based on the cited reference.

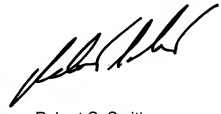
The allowed claims are again noted.

It is respectfully submitted that the now rejected claims (including withdrawn claims) are allowable and such action is requested.

A replacement sheet on which Fig. 2 appears is provided herewith. The legend "PRIOR ART" has been added to comply with the Examiner's requirement.

Should a petition for an Extension of Time be necessary for the timely reply to the outstanding office action (or such a petition has been made and an additional extension is necessary) petition is hereby made in the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account Number 19-2635 under Attorney Docket Number H0006069-0555.

Respectfully submitted,



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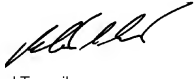

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